正基科技股份有限公司

AMPAK Technology Inc.

AP6398P

Evaluation Board User Manual

Address:
3F, No.15-1, Zhonghua Road, Hsinchu Industril Park, Hukou, Hsinchu,
Taiwan, 30352
Website: http://www.ampak.com.tw/

Revision

Revision	Date	Description	Revised By
1.0	2018/ 01 / 31	Initial released	Jerry Wu
1.1	2019/ 05 / 28	- Update user manual	Jerry Wu

Contents

1. EVB Introduction

AP6398P Evaluation board (EVB) likes as figure1. That is designed for IEEE802.11 a/b/g/n/ac 2x2 WLAN with integrated Bluetooth application. It is subject to provide a convenient environment for customer's verification on WiFi or Bluetooth function. There are many controller pins and reserved GPIO on Evaluation board which describes as below.

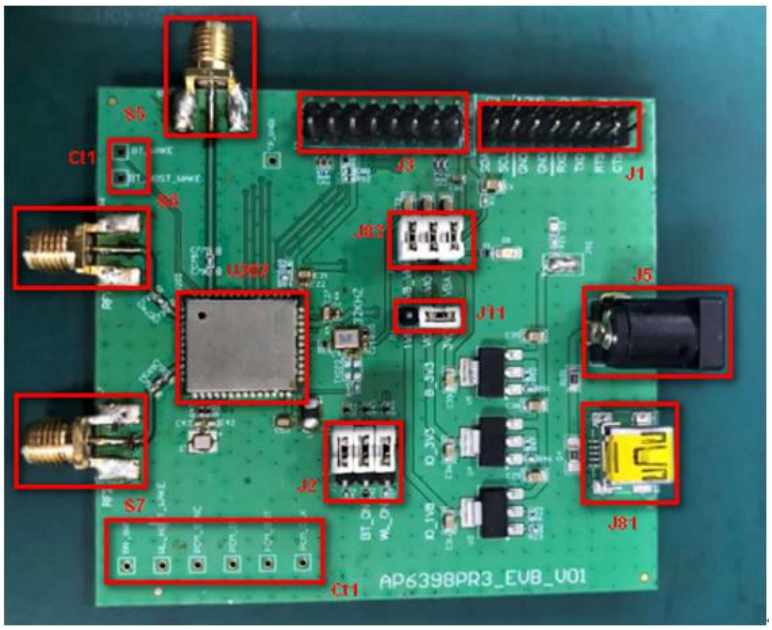

Figure1. Top view of AP6398P EVB

Interface highlights:

1. U202: AP6398P SIP module.
2. J1: UART interface connects with UART transport board for BT measuring
3. J2: Enable(H) or disable(L) Bluetooth, WiFi function
4. J83: VBAT / WL_VIO / BT_VIO for main system I/O power path.
5. J81: 5V DC mini USB input connector.
6. J3: PCIE interface connects with PCIE transport board for WIFI.
7. S6: SMA connector let WIFI RF signal in/out path,AP6398P BT signal in/out path, you could connect with RF cable or Dipole antenna.
8. S7: SMA connector let RF ANT2 signal in/out path, you could connect with RF cable or Dipole antenna.
9. Ct1: WLAN and BT control pins, strongly recommended WL_HWAKE(IRQ) connected to MCU.
10. J11: WL_VIO power path for 1V8 or 3V3 selection.

2. WiFi Function Verification Step

2.1 WiFi PCIE

PCIe interface definition as below J3 dip connector and this should be used 3.3V for PCIe voltage.

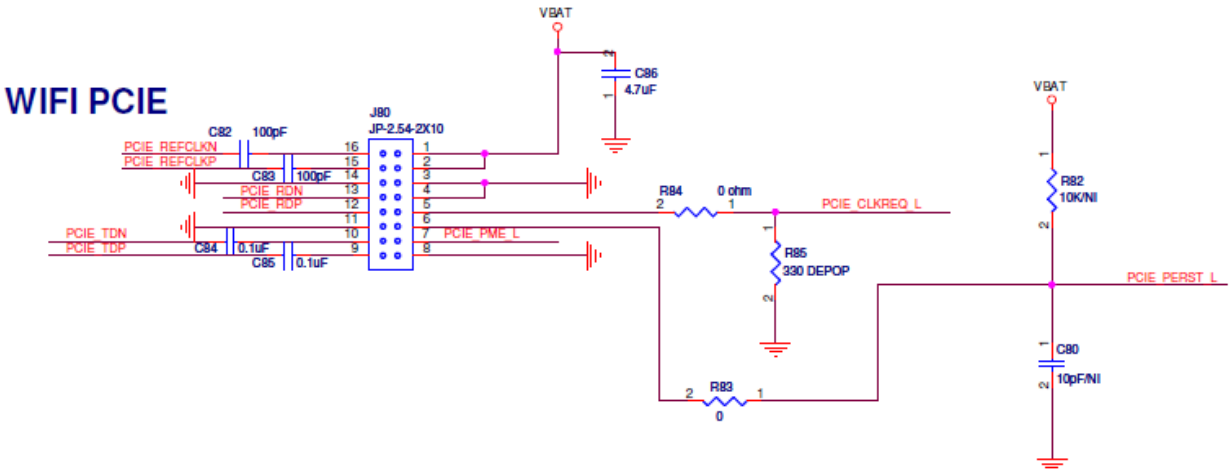

Figure2. WiFi verification connection interface to Host PCIE

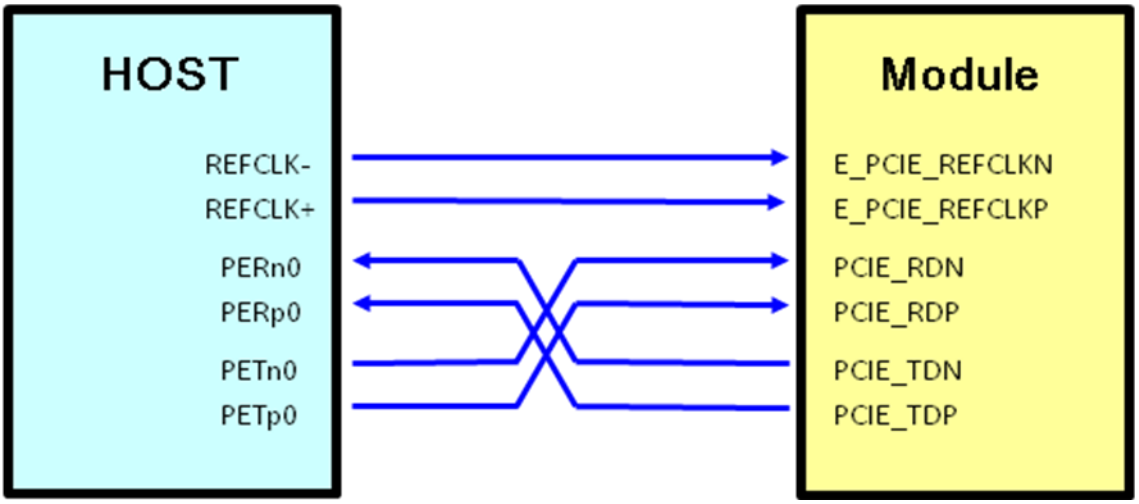

Figure3. EVB PCIE interface to HOST PCIE

2.2 Hardware Setup

- Refer to Figure2 PCIE pin definition connects the J3 interface of AP6398P evaluation board to Host PCIE control interface.
- Connects an external antenna at SMA connector on the evaluation board.
- Note to the VDDIO voltage level should be the same with GPIO voltage level of Host CPU. (VDDIO 3.3V or 1.8V selection by jump J11)

2.3 WiFi Software Setup

- Please follow up software guideline of Ampak official released.

3. Bluetooth Function Verification Step

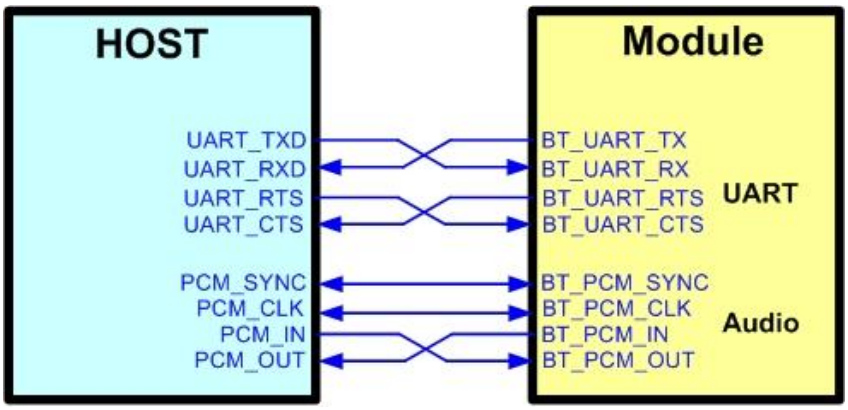

Figure4. Bluetooth verification connection interface to Host UART

Hardware Setup:

- Refer to Figure5 UART pin definition connects the J1 interface of AP6398P evaluation board to Host UART control interface.
- Connects an external antenna at SMA connector on the evaluation board.
- Note to the VDDIO voltage level should be the same as GPIO voltage level of Host CPU.

WiFi and Bluetooth software setup:

- Please follow up software guideline of Ampak official released.